Gaining Insight into Parallel Program Performance using HPCToolkit

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http://hpctoolkit.org



Challenges for Computational Scientists

- Rapidly evolving platforms and applications
 - architecture
 - rapidly changing multicore microprocessor designs
 - increasing architectural diversity
 CPU, GPU, APU, manycore (e.g., Xeon Phi)
 - increasing scale of parallel systems
 - applications
 - augment computational capabilities
- Computational scientist needs
 - adapt to changes in emerging architectures
 - adding threading and/or offloading to accelerators
 - improve scalability within and across nodes
 - assess weaknesses in algorithms and their implementations

Performance tools can play an important role as a guide

Performance Analysis Challenges

- Complex node architectures are hard to use efficiently
 - multi-level parallelism: multiple cores, ILP, SIMD, accelerators
 - multi-level memory hierarchy
 - result: gap between typical and peak performance is huge
- Complex applications present challenges
 - measurement and analysis
 - understanding behaviors and tuning performance
- Supercomputer platforms compound the complexity
 - unique hardware & microkernel-based operating systems
 - multifaceted performance concerns
 - computation
 - data movement
 - communication
 - **I/O**

What Users Want

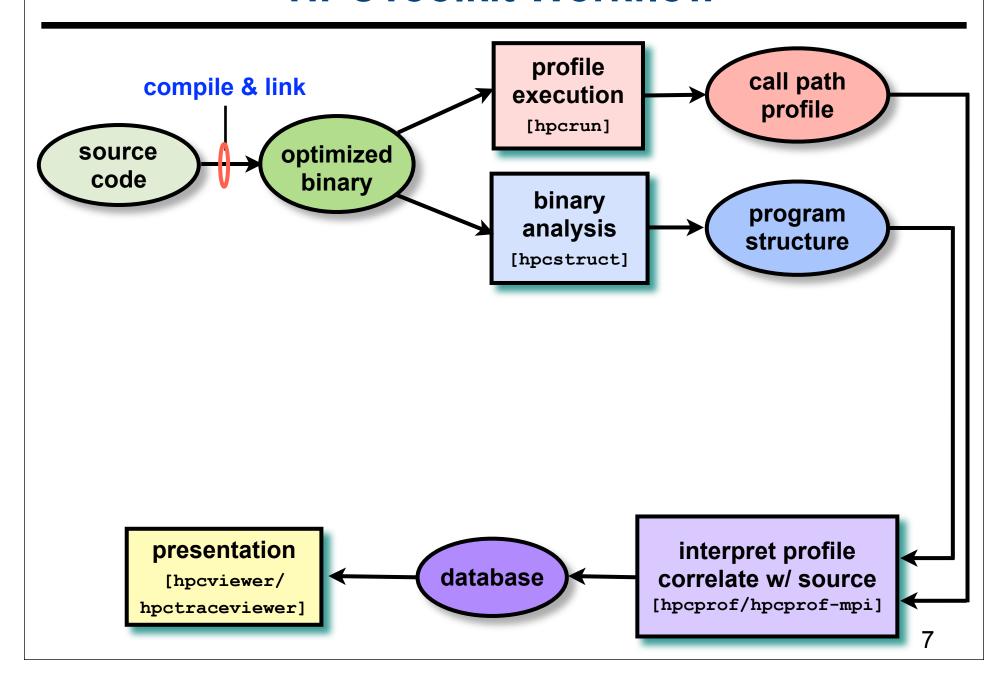
- Easy-to-use multi-platform, programming model independent tools
- Accurate measurement of complex parallel codes
 - large, multi-lingual programs
 - (heterogeneous) parallelism within and across nodes
 - optimized code: loop optimization, templates, inlining
 - binary-only libraries, sometimes partially stripped
 - complex execution environments
 - dynamic binaries on clusters; static binaries on supercomputers
 - batch jobs
- Effective performance analysis
 - insightful analysis that pinpoints and explains problems
 - correlate measurements with code for actionable results
 - support analysis at the desired level
 intuitive enough for application scientists and engineers
 detailed enough for library developers and compiler writers
- Scalable to petascale and beyond

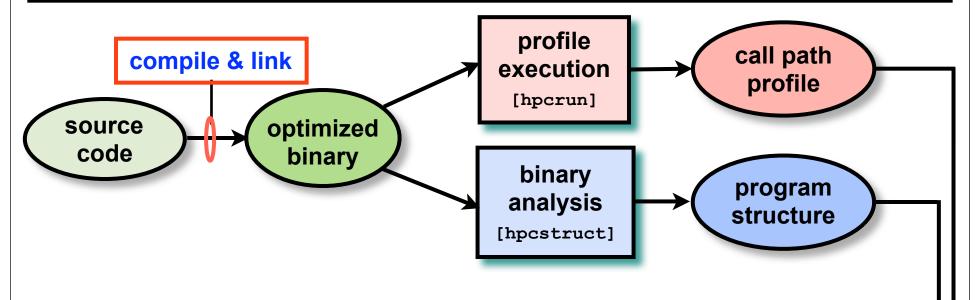
Rice University's HPCToolkit

- Employs binary-level measurement and analysis
 - observe executions of optimized code
 - support multi-lingual codes with external binary-only libraries
- Uses sampling-based measurement (avoid instrumentation)
 - controllable overhead
 - minimize systematic error and avoid blind spots
 - enable data collection for large-scale parallelism
- Collects and correlates multiple derived performance metrics
 - diagnosis typically requires more than one species of metric
- Associates metrics with both static and dynamic context
 - loop nests, procedures, inlined code, calling context
- Supports top-down performance analysis
 - natural approach that minimizes burden on developers

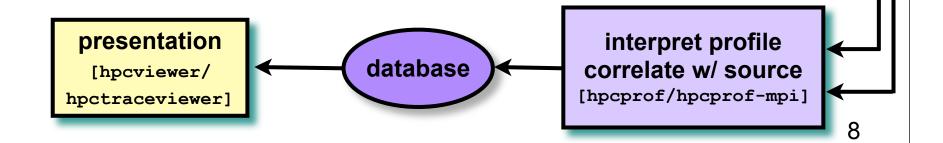
Outline

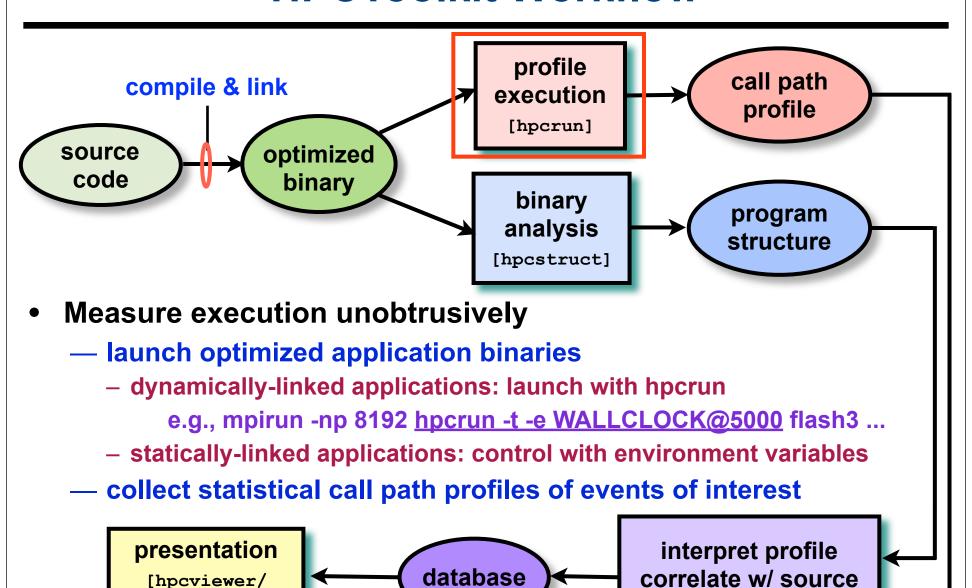
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- For dynamically-linked executables, e.g., Linux
 - compile and link as you usually do
- For statically-linked executables, e.g., Blue Gene/Q
 - add monitoring by using hpclink as prefix to your link line





[hpcprof/hpcprof-mpi]

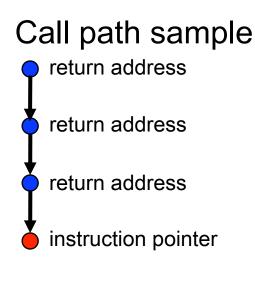
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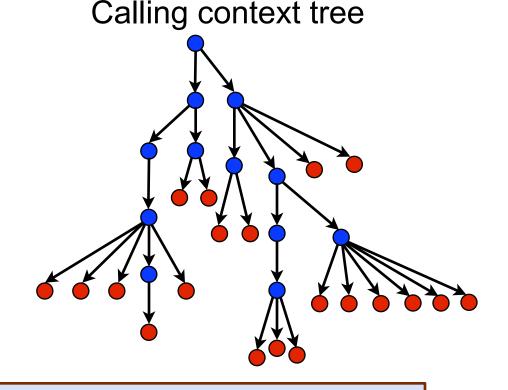
hpctraceviewer]

Call Path Profiling

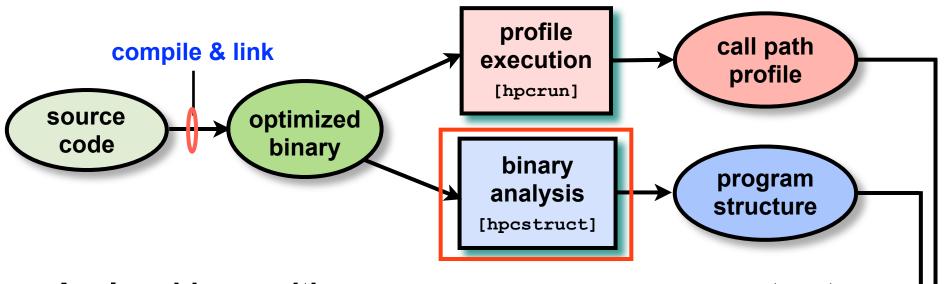
Measure and attribute costs in context

sample timer or hardware counter overflows gather calling context using stack unwinding

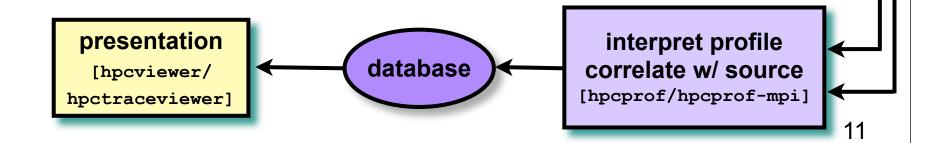


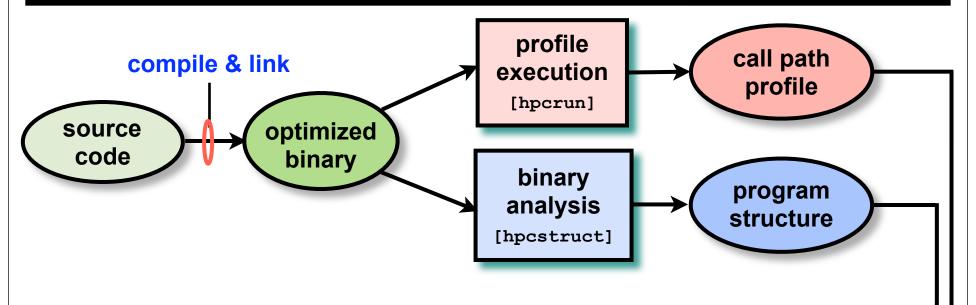


Overhead proportional to sampling frequency...
...not call frequency

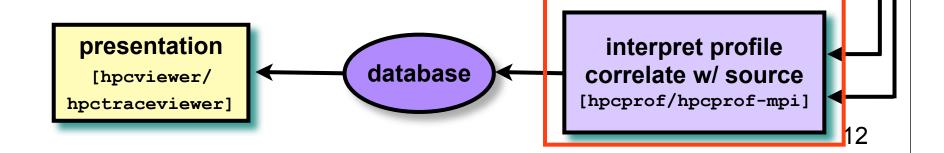


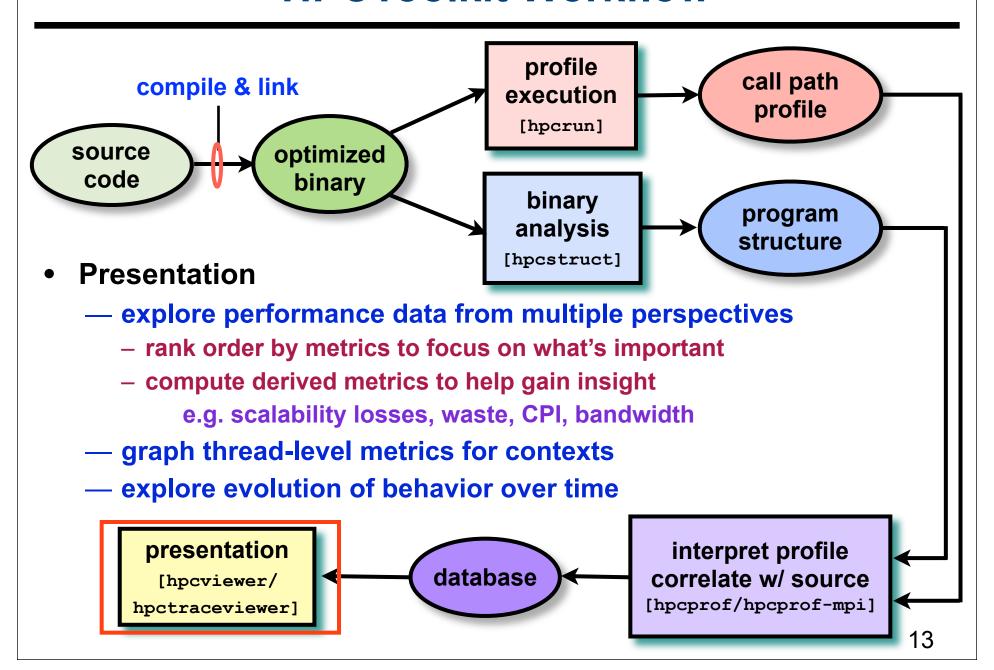
- Analyze binary with hpcstruct: recover program structure
 - analyze machine code, line map, debugging information
 - extract loop nesting & identify inlined procedures
 - map transformed loops and procedures to source



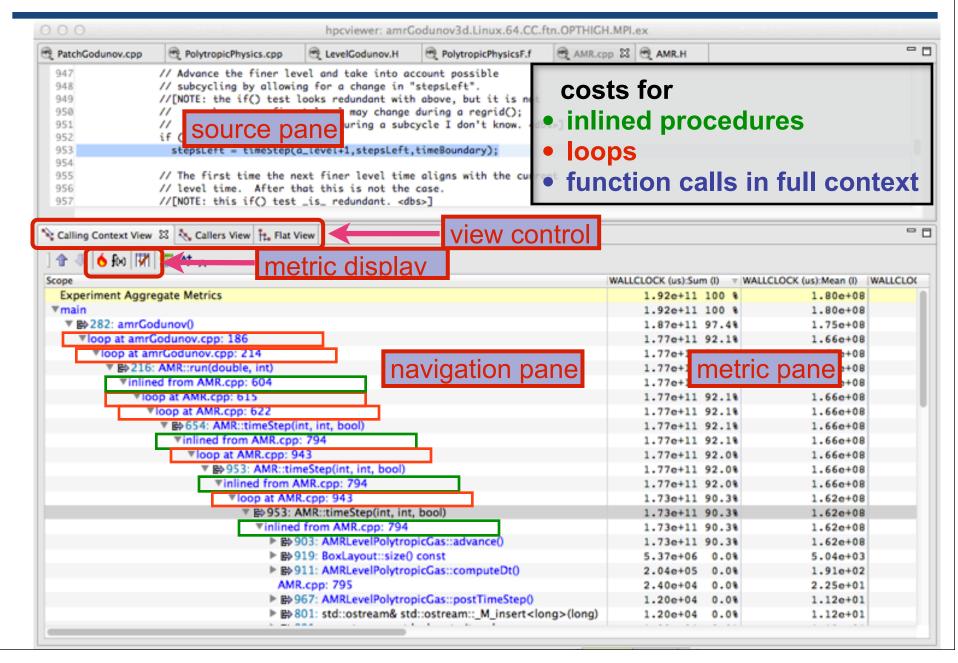


- Combine multiple profiles
 - multiple threads; multiple processes; multiple executions
- Correlate metrics to static & dynamic program structure





Analyzing Chombo@1024 cores with hpcviewer



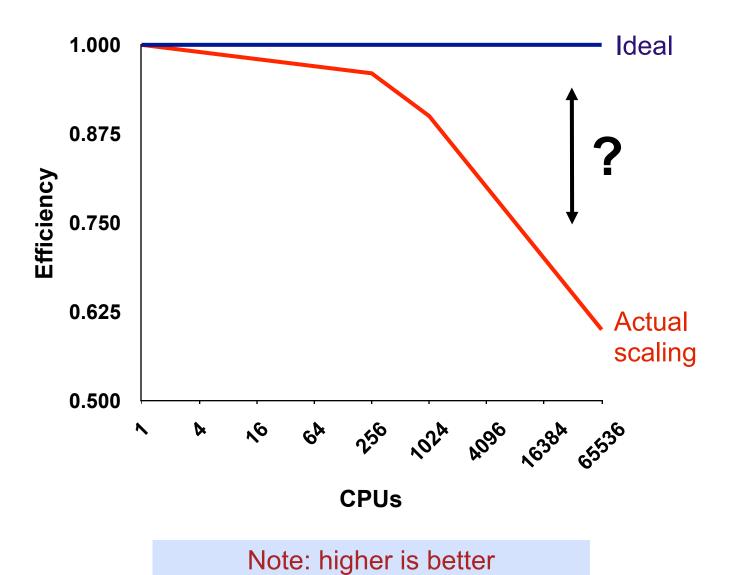
Principal Views

- Calling context tree view "top-down" (down the call chain)
 - associate metrics with each dynamic calling context
 - high-level, hierarchical view of distribution of costs
 - example: quantify initialization, solve, post-processing
- Caller's view "bottom-up" (up the call chain)
 - apportion a procedure's metrics to its dynamic calling contexts
 - understand costs of a procedure called in many places
 - example: see where PGAS put traffic is originating
- Flat view ignores the calling context of each sample point
 - aggregate all metrics for a procedure, from any context
 - attribute costs to loop nests and lines within a procedure
 - example: assess the overall memory hierarchy performance within a critical procedure

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The Problem of Scaling



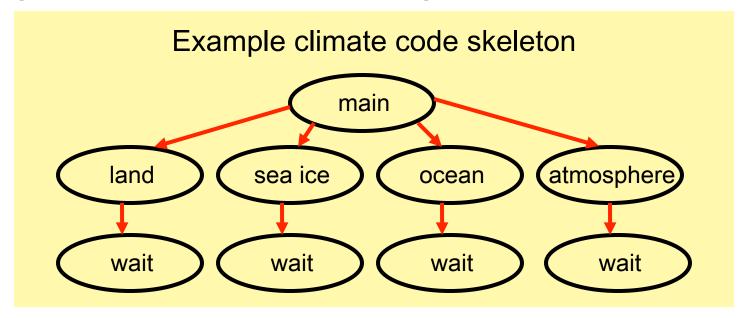
Wanted: Scalability Analysis

- Isolate scalability bottlenecks
- Guide user to problems
- Quantify the magnitude of each problem

Challenges for Pinpointing Scalability Bottlenecks

Parallel applications

- modern software uses layers of libraries
- performance is often context dependent



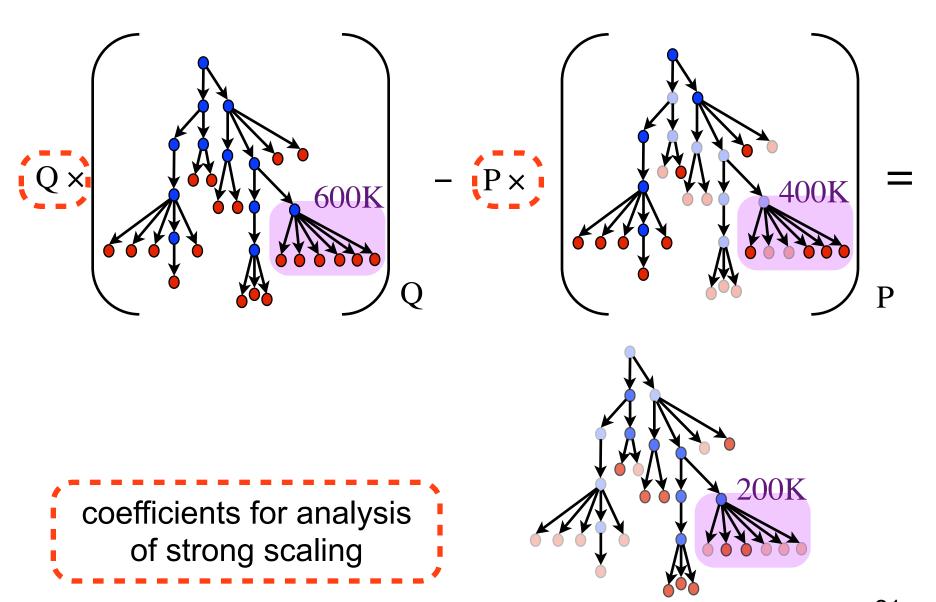
Monitoring

- bottleneck nature: computation, data movement, synchronization?
- 2 pragmatic constraints
 - acceptable data volume
 - low perturbation for use in production runs

Performance Analysis with Expectations

- You have performance expectations for your parallel code
 - strong scaling: linear speedup
 - weak scaling: constant execution time
- Put your expectations to work
 - measure performance under different conditions
 - e.g. different levels of parallelism and/or different problem size
 - express your expectations as an equation
 - compute the deviation from expectations for each calling context
 - for both inclusive and exclusive costs
 - correlate the metrics with the source code
 - explore the annotated call tree interactively

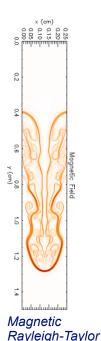
Pinpointing and Quantifying Scalability Bottlenecks



Scalability Analysis Demo: FLASH3

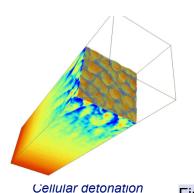
Code:
Simulation:
Platform:
Experiment:
Scaling type:

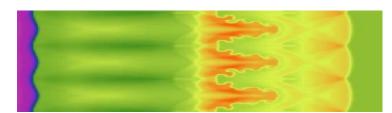
University of Chicago FLASH3 white dwarf detonation Blue Gene/P 8192 vs. 256 processors weak



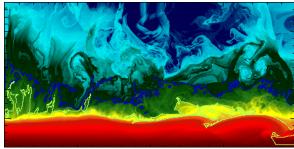


Nova outbursts on white dwarfs

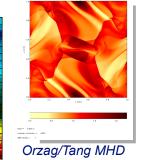




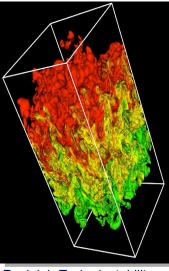
Laser-driven shock instabilities



Helium burning on neutron stars



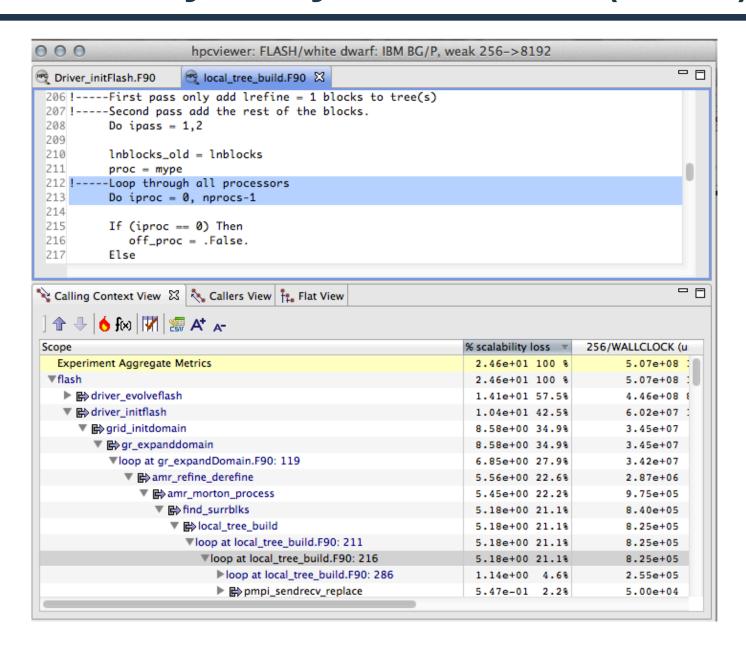
Orzag/Tang MHD vortex



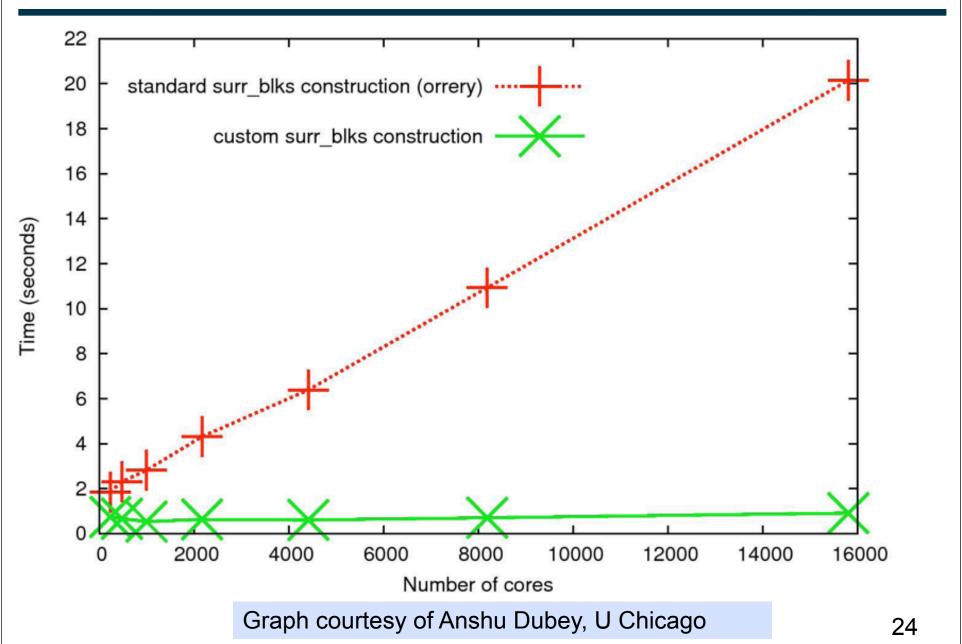
Rayleigh-Taylor instability

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Scalability Analysis of Flash3 (Demo)



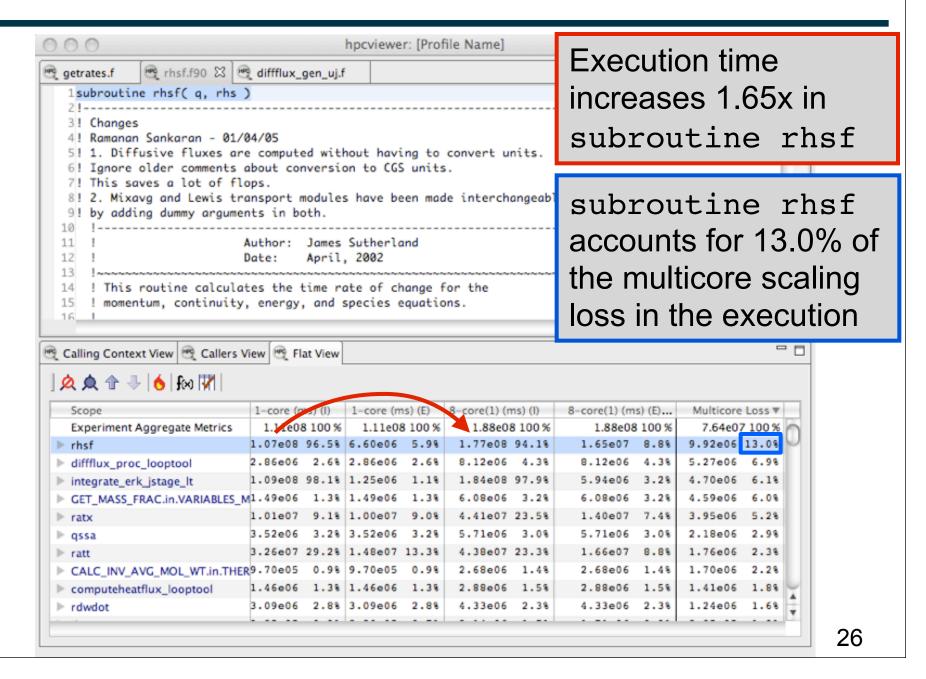




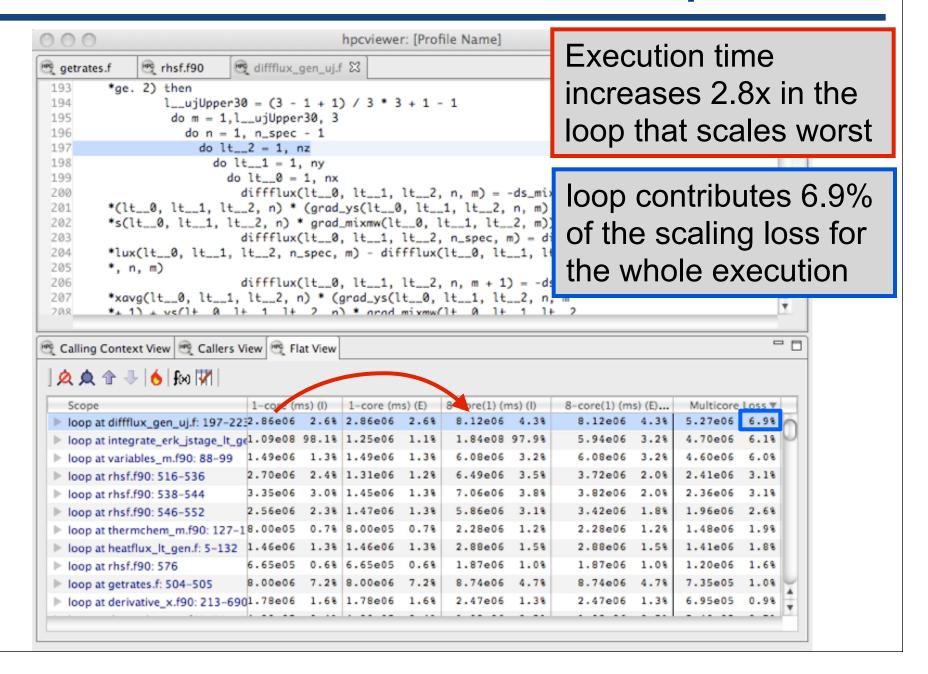
Scaling on Multicore Processors

- Compare performance
 - single vs. multiple processes on a multicore system
- Strategy
 - differential performance analysis
 - subtract the calling context trees as before, unit coefficient for each

S3D: Multicore Losses at the Procedure Level



S3D: Multicore Losses at the Loop Level



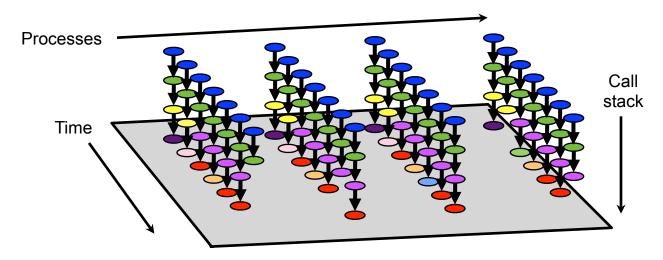
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Understanding Temporal Behavior

- Profiling compresses out the temporal dimension
 - —temporal patterns, e.g. serialization, are invisible in profiles
- What can we do? Trace call path samples
 - -sketch:
 - N times per second, take a call path sample of each thread
 - organize the samples for each thread along a time line
 - view how the execution evolves left to right
 - what do we view?

assign each procedure a color; view a depth slice of an execution

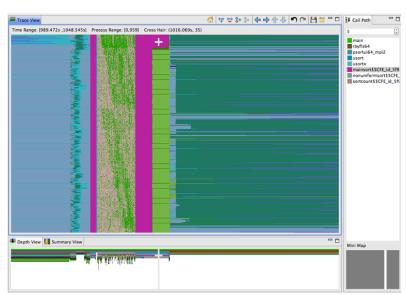


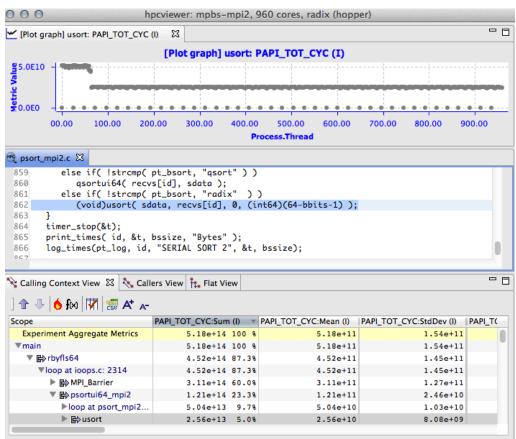
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MPBS @ 960 cores, radix sort

Two views of load imbalance since not on a 2^k cores





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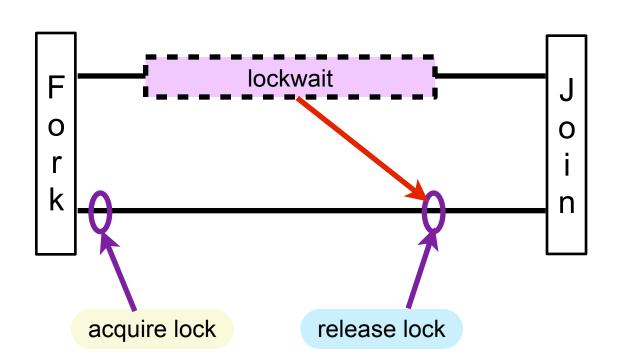
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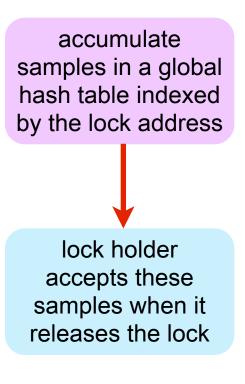
Blame Shifting

- Problem: in many circumstances sampling measures symptoms of performance losses rather than causes
 - worker threads waiting for work
 - threads waiting for a lock
 - MPI process waiting for peers in a collective communication
 - idle GPU waiting for work
- Approach: shift blame for losses from victims to perpetrators
 - blame code executing while other threads are idle
 - blame code executed by lock holder when thread(s) are waiting
 - blame processes that arrive late to collectives
 - shift blame between CPU and GPU for hybrid code

Directed Blame Shifting

- Example:
 - threads waiting at a lock are the symptom
 - the cause is the lock holder
- Approach: blame lock waiting on lock holder





Example: Directed Blame Shifting for Locks

- 0

almost all blame

for the waiting is

MUTEX BLAME:Sum (I)

7.93e+07 100 %

attributed here

(cause)

MUTEX_WAIT:Sum (I)

8.11e+07 100 %

hpcviewer: locktest-2.host

3 void g() { 4 int i;

10

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File View Window Help

1 #include <omp.h> 2 #include "fib.h"

omp lock t l;

omp_init_lock(&l);

fib(40);

#pragma omp parallel

#pragma omp master

omp_set lock(&l);

Blame a lock holder for delaying waiting threads

 Charge all samples that threads receive while awaiting a lock to the lock itself

occurs

(symptom

here

 When releasing a lock, accept blame at all of the lock the waiting

#pragma omp for $for(i = 0; i < 100; i++) {$ omp set lock(&l); fib(10): omp unset lock(&l); 21 } 22 } 23 void f() { g(); } 24 int main() { f(); return 0; } 🔖 Calling Context View 🛭 🛝 Callers View 🛼 Flat View Scope Experiment Aggregate Metrics monitor main ¬ □ 7: L g 7 par region0 2 90 ▶ № 17: kmpc set lock

▷ B⇒ 12: fib

▶ 20: __kmpc_barrier

Undirected Blame Shifting

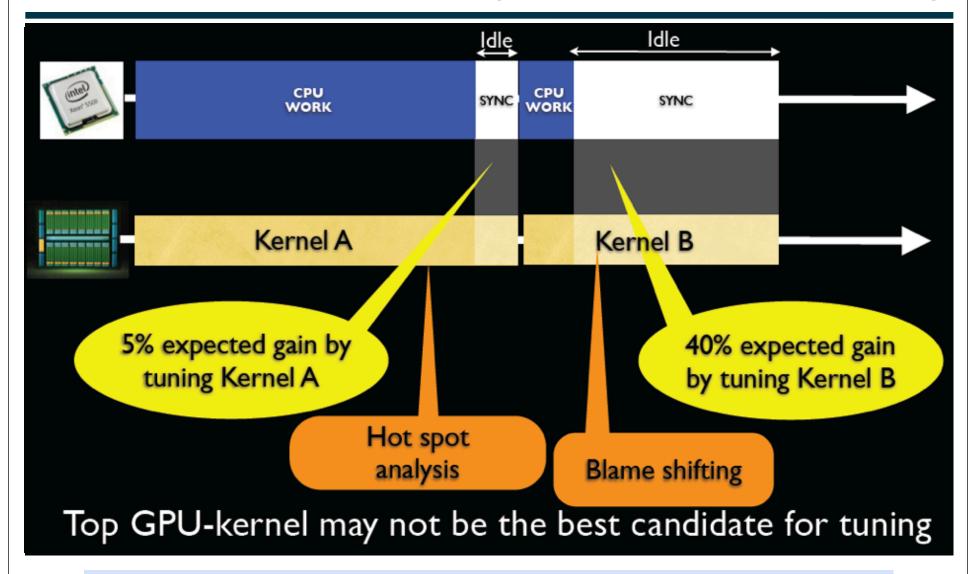
- Example:
 - threads idling waiting for work are the symptom
 - the cause is insufficiently parallel work being executed by others
- Approach: each working threads proportionally blames itself for instantaneous idling by others when it is sampled



counters hold the number of threads working and idle

working thread charges itself a share of idleness at each sample

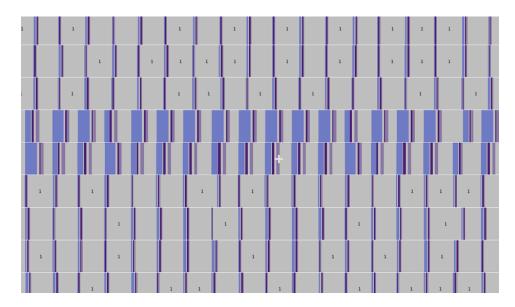
Performance Expectations for Hybrid Code with Blame Shifting



Milind Chabbi, Karthik Murthy, Michael Fagan, and John Mellor-Crummey. Effective Performance Tools for CPU/GPU Systems. SC13. To appear.

GPU Successes with HPCToolkit

- LAMMPS: identified hardware problem with Keeneland system
 - improperly seated GPUs were observed to have lower data copy bandwidth



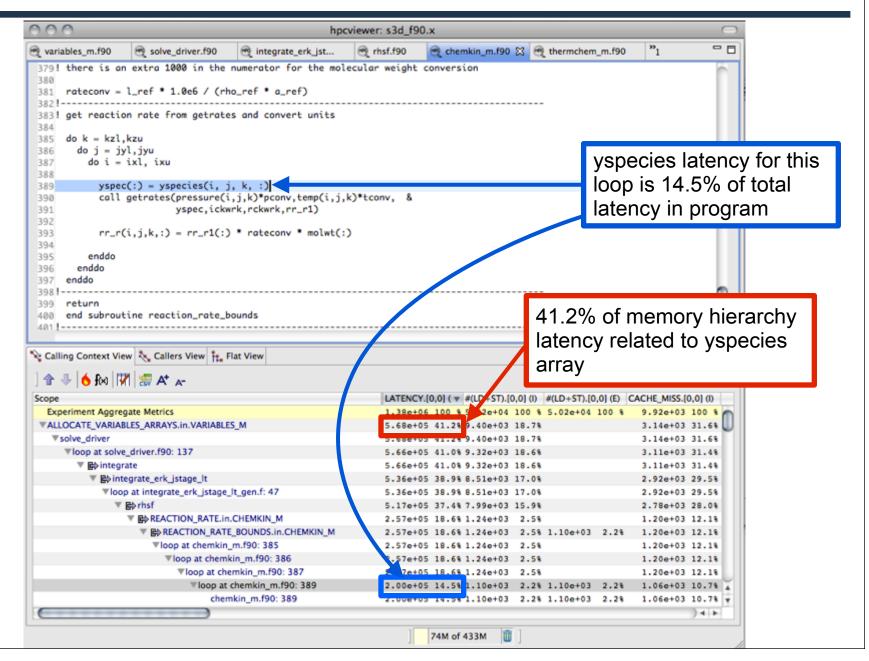
 LLNL's LULESH: identified that dynamic memory allocation using cudaMalloc and cudaFree accounted for 90% of the idleness of the GPU

Data Centric Analysis

- Goal: associate memory hierarchy performance losses with data
- Approach
 - intercept allocations to associate with their data ranges
 - measure latency with various PMU capabilities
 - instruction-based sampling (AMD Opteron)
 - precise event-based sampling + load latency facility (Intel)
 - marked instructions (IBM Power)
 - present quantitative results using hpcviewer

Xu Liu and John Mellor-Crummey. A Data-centric Profiler for Parallel Programs. SC13. To appear.

Data Centric Analysis of S3D



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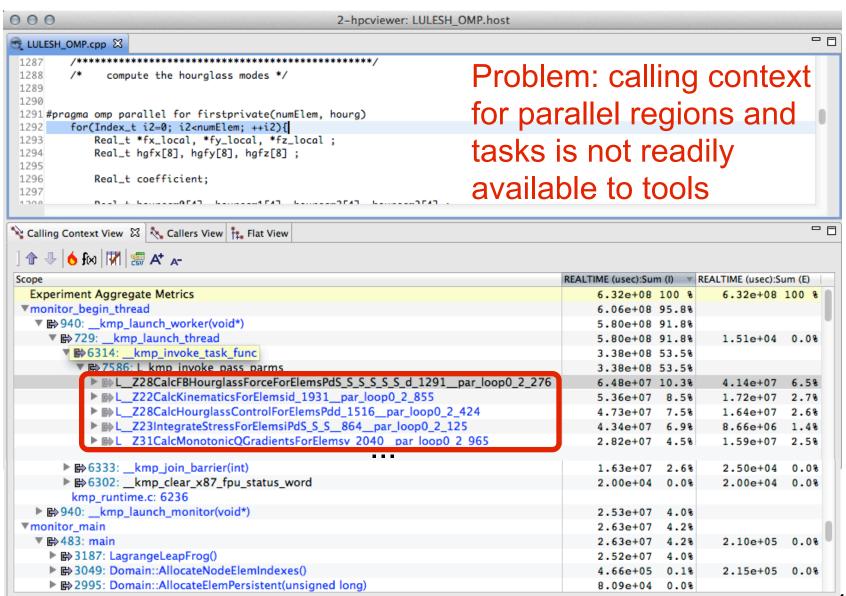
Summary

- Sampling provides low overhead measurement
- Call path profiling + binary analysis + blame shifting = insight
 - scalability bottlenecks
 - where insufficient parallelism lurks
 - sources of lock contention
 - load imbalance
 - temporal dynamics
 - bottlenecks in hybrid code
 - problematic data structures
 - hardware counters for detailed diagnosis
- Other capabilities
 - attribute memory leaks back to their full calling context

HPCToolkit Status

- Operational today on
 - 64- and 32-bit x86 systems running Linux (including Cray XT/E/K)
 - IBM Blue Gene
 - IBM Power7 systems running Linux
- Available as open source software at http://hpctoolkit.org
- Emerging capabilities
 - NVIDIA GPU
 - measurement and reporting using GPU hardware counters
 - data centric analysis
 - OpenMP analysis using OMPT

OMPT: Emerging Monitoring for OpenMP

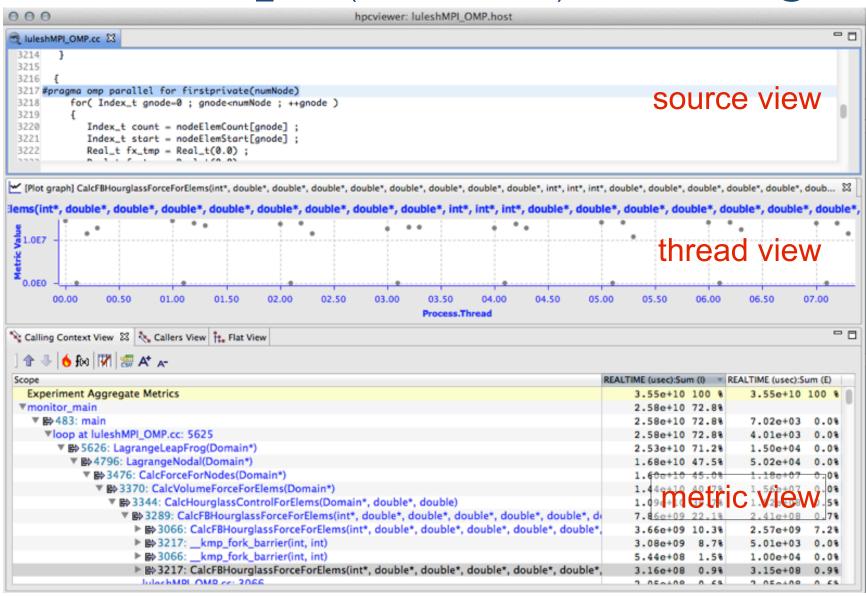


Key OMPT Design Objectives

- Enable tools to gather information and associate costs with application source and runtime system
 - provide interface for low-overhead sampling-based tools
 - enable tools to reconstruct application-level profiles
 - alternative to implementation-level view
 - associate activity of a thread at any point in time with a state
 - enable performance tools to monitor behavior
- Negligible overhead if OMPT interface is not in use
- Define support for trace-based performance tools

Integrated View of MPI+OpenMP with OMPT

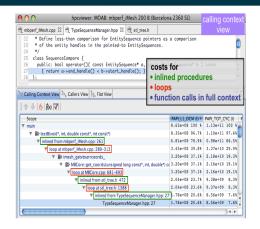
LLNL's luleshMPI_OMP (8 MPI x 3 OMP), 30, REALTIME@1000



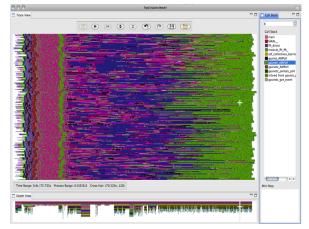
Tool Challenges Ahead

- Address challenges of emerging systems
 - heterogeneity (e.g., on-chip; host + accelerator)
 - growth in thread counts: MIC supports 200+ threads
 - increasing scale of systems (e.g., Sequoia)
- Identify <u>causes</u> rather than <u>symptoms</u> (blame shifting)
- Measure and analyze all facets of application performance
 - CPU, accelerator, data movement, synchronization, I/O, power
 - interactions: HW, other jobs, system software
- Analyze asynchronous activities
- Support dynamic adaptation of software
 - measurements and decision algorithms to drive adaptation
 - assessment of adaptation policies
- Provide analysis to support higher level insight, diagnosis, and guidance

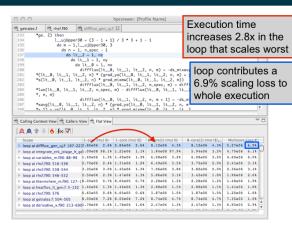
HPCToolkit Capabilities at a Glance



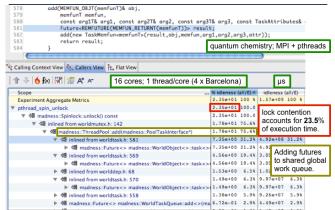
Attribute Costs to Code



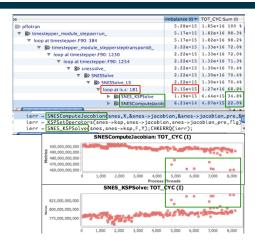
Analyze Behavior over Time



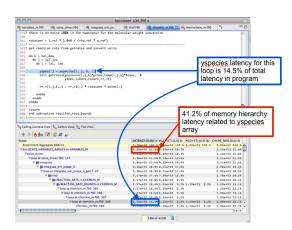
Pinpoint & Quantify Scaling Bottlenecks



Shift Blame from Symptoms to Causes



Assess Imbalance and Variability



Associate Costs with Data

hpctoolkit.org

